PROCESS AND DEVICES FOR TRANSMITTING DIGITAL SIGNALS OVER BUSES AND COMPUTER PROGRAM PRODUCT THEREFORE

BACKGROUND OF THE INVENTION

Field of the invention

The present invention relates to techniques for encoding data and tackles in a specific way the problem of encoding digital signals that are to be transmitted on a bus, the chief purpose being to reduce the transitions of the signal levels on the bus, i.e., what, in the sector is generally referred to as "switching activity" (SA).

Description of the Related Art

To reduce transitions, and consequently switching activity on buses, a known solution is to resort to various encoding techniques. The technique currently referred to as the bus-inverter (BI) technique is considered the solution most suitable for buses of small size, for example of up to 8 bits, even though the results may vary according to the type of data processed.

The bus-inverter technique implements an encoding based upon the logical inversion of the bits of the signals transmitted and uses an additional bus-line, designated by INV, to indicate to the receiver whether the datum sent is inverted or not.

Designated by D(t) is the datum that it is intended to transmit and by B(t) the corresponding datum that travels on the bus at a generic instant in time t. The working principle underlying the bus-inverter technique is essentially represented by the logic expression:

$$(B(t), INV(t)) = (D(t), 0) \text{ if } H(D(t), B(t-1)) \leq n/2$$

$$(NOT(D(t)), 1) \text{ in the other cases.}$$

In the expression appearing above, n indicates the dimension of the bus expressed in number of bits, whilst the operator H(.) indicates a distance operator, such as, for example, the Hamming distance. The symbol NOT(.) indicates of course the logic-inversion operation ($0 \rightarrow 1$, $1 \rightarrow 0$).

Basically, the decision as regards whether to invert or not to invert the datum is taken by calculating the distance between the datum D(t) that it is intended to send at the instant t and the datum B(t–1) used for transmission on the bus for the preceding instant of transmission.

The technique described above is used also in variants like the one referred to as "Adapted Partial Bus Inverter" (APBI). With this technique, developed above all for use on buses of large dimensions, the number of bits to which the bus-inverter technique is to be applied is reduced by means of masks. These are masks that are kept fixed for an entire transmission window and calculated by means of an estimate made on the type of data to be transmitted. This involves considerable processing times and the need to resort to a circuit of a rather complicated type for the calculation/estimation of the mask.

BRIEF SUMMARY OF THE INVENTION

The present invention improves upon the techniques described above.

The invention also regards the corresponding encoding and decoding devices, as well as the corresponding computer products, which are directly loadable into the internal memory of a computer and comprise portions of software code that are able to implement the procedure and/or the devices according to the invention when said computer products are run on a computer.

An embodiment of the invention verifies occurrence of a condition in which transmission in non-encoded format and transmission in encoded format are liable to give rise to an identical switching activity on the bus, the aim being to choose the format (non-encoded/encoded) to be transmitted in such a way as to

cause the associated additional signal (INV), designed to indicate the presence or absence of encoding, to preserve its previous logic value without being subject to transition.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described, purely by way of non-limiting example, with reference to the annexed drawings, in which:

Figure 1 is a flowchart illustrating transmission of digital signals on a bus;

Figure 2 is a another flowchart illustrating transmission of digital signals on a bus;

Figure 3 represents, in the form of a block diagram, a corresponding encoder/bus/decoder system;

Figure 4 is a block diagram corresponding to an encoder that can be comprised in a system such as the system represented in Figure 3;

Figures 5, 6, 7 and 8 represent, in greater detail, elements comprised in the diagram of Figure 4;

Figure 9 represents the structure of a decoder that can be comprised in a system such as the system represented in Figure 3;

Figures 10 to 13 represent, resorting to representations corresponding to the representations of Figures 4, 5, 8 and 9, respectively, a possible variant embodiment of the invention; and

Figure 14 is a flowchart illustrating operation of an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The flowchart of Figure 1 illustrates a first encoding solution applicable to a datum D(t) designed to be transmitted on a bus P (Figure 3), and

B(t) designates, as a whole, the corresponding signal actually transmitted on the bus P.

The foregoing is with reference to an instant in time t.

Consequently, by B(t–1) is designated the signal used for the transmission on the bus for a preceding instant in time, indicated by t–1. In practice B(t–1) is the value that can be found on the bus when it is necessary to transmit D(t).

The datum D(t) is made up of n bits (D_{n-1}, D_{n-2} ..., D_1, D_0), whilst the bus P comprises n+1 bits: the bus comprises, in fact, also the line for the transmission of an additional signal INV designed to indicate whether the datum transmitted on the bus has undergone inversion (or, in general, encoding) in order to minimize the switching activity (SA) on the bus P.

As has been seen previously, with the bus-inverter technique of a traditional type, the datum is encoded (i.e., subjected to inversion on all the bits that make it up) if the distance between the signal D(t) and the signal B(t–1), detected on all the n bits, is less than n/2.

Instead, in a first example of embodiment of the technique described herein, starting from a start step designated by 100, in a step designated by 102 the procedure starts from the most significant bit (MSB) of D(t), referred to as $D_{n-1}(t)$, which is sent without encoding on the bus in a step designated in general by 104.

In a next step, 106, a check is then made to determine whether $D_{n-1}(t)$ is equal to the most significant bit of B(t–1), namely $B_{n-1}(t-1)$.

If equality is found (positive outcome from step 106), then the system goes to step 108, in which the index i is decremented, and the sequence of steps 104 and 106 seen previously is repeated with the decremented index.

This mode of procedure is equivalent to making, according to an orderly sequence (for example, starting from the most significant bit), a comparison, bit by bit, between D(t) and B(t–1). This is done by taking, one after

another, the various bits of the datum D(t), proceeding in orderly sequence from the most significant bit to the least significant bit and continuing to send, on the bus P, the bits of D(t), without encoding, until, in step 106, identity between the bit of the signal or datum D(t) and the corresponding bit of the signal B(t–1) considered each time for the comparison a continues to be found.

As soon as an inequality is found (which, it is emphasized, may occur even at the first execution of the step 106), the bit in which the inequality occurs is assumed as marker bit, and the system goes to a step 110 of decrement of the current index i, and then proceeds, in a step designated by 112, to the encoding (for example using the bus-inverter technique of a traditional type) of the subset of remaining bits.

One of skill in the art, after review of the specification, will recognize that additional factors may be employed in deciding whether to encode a given bit in a digital signal. For example, the datum may be encoded when the aforesaid distance value H is less than M/2, where M is the position (from 0 to n–1) of the marker bit identified in the step designated by 106, but not encoded when the distance value is equal to or greater than M/Z.

With the technique described herein, for M other than (n–1) a switching activity less than or equal to that of the bus-inverter technique of a traditional type may be achieved. However, for M=(n–1), the switching activity with the solution described herein may be greater than 1 as compared to that of the bus-inverter technique of a traditional type. The particular case M=(n–1) is found, however, only in the case where the most significant bit of the datum D changes with respect to the current value on the bus P.

The experience deriving from a practical application of the embodiment described previously shows that, with a configuration or pattern of data considered in a random manner, the embodiment just described in any case enables a reduction of the switching activity SA in the region of 51% as compared to the results obtainable using the bus-inverter technique of a traditional type.

In the presence of particular configurations of data (for example, data that represent a digital ramp i.e., a number increasing from 0 to 255), the embodiment just described enables a reduction in the switching activity to be obtained in the region of 83% as compared to the bus-inverter technique of a traditional type.

A further improvement may be achieved by resorting to the variant embodiment represented in Figure 2.

Basically, the embodiment of Figure 2 handles the case of M=n–1 apart, distinguishing it from the cases in which M<n–1 and applying in the first case a technique of a traditional type and in the other cases the embodiment described previously with reference to Figure 1.

The adoption of the embodiment according to Figure 2 involves transmission of the further information. This may be done using a three-level signal INV, for example 0, 0.5 and 1, and encoding, in an optimal way, the value 0 for the non-encoding, the value 0.5 for the encoding in the case of the innovative solution described herein, and the value 1 for encoding of a traditional type, *i.e.*, the inversion of the whole datum because M=n–1. Inversion of the datum, i.e., its encoding, is preferably performed only in the case where the encoded case transmitted on the bus has a switching activity less than its non-encoded value.

Also in this case, D designates the datum that is to be sent and B the datum that is actually transmitted on the bus.

Consequently, D(t) identifies the datum that is to be sent at the instant t, whilst B(t–1) is the datum actually transmitted, corresponding to the instant t–1, i.e., in practice, the value that is found on the bus when it is necessary to transmit D(t). As in the preceding case, B(t) represents the expression of the datum D(t) actually encoded used for transmission on the bus at the instant t.

Also in this case it is assumed that the datum D(t) is made up of n bits and the bus P consists of n+1 bits, taking into account the additional bit required for the signal INV.

In the flowchart of Figure 2, steps that are identical or equivalent to the ones already described with reference to Figure 1 are designated using the same reference numbers.

Also in the case of the embodiment represented in Figure 2, starting from a start step designated by 100, in step 102 the most significant bit of D(t) is identified, and the process then passes on to a first comparison step 106' reserved to the aforesaid most significant bit, aimed at verifying whether the said most significant bit $D_{n-1}(t)$ is equal to the most significant bit of B(t–1) , i.e., $B_{n-1}(t-1)$.

If the step 106' yields a positive result, indicating the fact that the two bits compared are equal, the bit involved is sent, just as it is, on the bus, there also being set, in a step designated by 114, a corresponding identifier flag (Flag=0).

At this point, there is cyclically set under way the sequence of steps 104, 106" and 108 according to the same modalities described previously in Figure 1, with the difference represented by the fact that the said sequence of steps is carried out (proceeding step by step towards the least significant bits), taking into account that the most significant bit has already been processed, apart, in the step designated by 106'.

Consequently, also in this case the bits of the signal D(t) are sent on the bus P just as they are, without them being encoded, i.e., without them being inverted, until the step 106" confirms the equality with the bits of B(t–1).

If, starting from a given bit, the step 106' yields a negative result, the corresponding bit becomes a marker bit, and the (sub)set of bits that remain is subjected to encoding (for example, being processed using the classic bus-inverter technique – step 112).

Direct evolution towards the step 112 is obtained, instead, already starting from step 106' in the case where the inequality is detected at the most significant bit. This corresponds to a negative result of the comparison step 106' and to the subsequent setting, in a step designated by 116, of a flag (Flag=1) with a value different from that of the flag (Flag=0) set in the step 114.

In step 112, there is also the generation of the bit INV according to the following law:

- if the signal D(t) is not – even partially – to be encoded, INV is set equal to 0,

- if it is necessary to encode, i.e., to invert (at least in part) the signal D(t), INV is set equal to 0.5 or equal to 1 according to whether the flag referred to above is set at 0 (step 114) or at 1 (step 116).

The variant embodiment represented in Figure 2 presents all the advantages of the embodiment already described previously with reference to Figure 1, with the additional advantage represented by the fact that, in the particular case of M=n–1, in any case also the reduction in the switching activity related to the most significant bit is recovered because we return to encoding of a traditional type (for example, using the bus-inverter technique).

The block diagram of Figure 3 illustrates the general structure of a system that is able to operate with the variants illustrated in Figures 1 and 2. Represented in the block diagram of Figure 3 are a circuit encoder 10 and a circuit decoder 20 set, respectively, at the input end and at the output end of a bus designated by P. The said bus P comprises, in general, n data bits (data bus) plus an additional bit for transmission of the signal INV (inv_bus).

The symbols DATA_IN and DATA_OUT of course indicate the input data and output data with respect to the transmission on the bus P. The said transmission occurs under the clocking of a clock signal clk sent both to the encoder 10 and to the decoder 20, under which there also comes a general reset line (reset).

The block diagram of Figure 4 represents an embodiment of the encoder 10 in greater detail.

The reference 11 designates a module designed to carry out the encoding of the datum to be transmitted (in practice, in the example to which reference is made herein, its logic inversion: $0 \rightarrow 1$, $1 \rightarrow 0$).

The blocks 12 and 13 carry out, both in an inverted connection and in a non-inverted connection, calculation of the Hamming distance between two strings of n bits.

The purpose of this is to detect the number of different bits between:

- the input datum D(t), represented by the signals data_in (non-inverted format) and data_invert (inverted format); and

- the datum used for transmission on the bus for the preceding instant, i.e., the value B(t–1) fetched from the output line data_out_encoder.

Block 14 compares the value of the two Hamming distances calculated in the modules 12 and 13 and indicates at output which of these has the lower value. The corresponding result is used for driving an n-bit multiplexer 15 designed to transfer to the output the non-inverted input signal, or the inverted input signal, received at output from the module 11 according to the outcome of the comparison made in block 14.

The reference numbers 16 and 17 indicate two flip-flops designed to implement physically the duration of the individual time interval that separates the instants designated, respectively, by t–1 and t.

In addition to representing the output of the encoder, the output of the flip-flop 17 is also brought back to the input of the blocks 12 and 13 according to the modalities described previously. The output of the flip-flop 16 is instead brought back to the input of the comparison module 14. The aim of this is that, if the two Hamming distances calculated in the modules 12 and 13 are found to be equal, the value of the bit INV to be sent on the bus will remain equal to the preceding one. In fact, in this case, it makes absolutely no difference whether the data is sent inverted or not on the bus, and hence the choice is determined by the preceding value of INV so as to prevent switching of said bit. As useful reference, the code of the algorithm of the block 14 in Figure 8 may be considered.

The diagram of Figure 5 represents, at the level of logic gates, a possible implementation of the module designated by 11 in Figure 4.

The reference numbers 1011, 1012 and 1013 represent respective arrays of logic gates of the EX–OR, AND (NAND) and again EX–OR types, which are designed to implement selectively the inversion of the bits of the input datum D(t) according to the value (detected bit by bit) of the signal data_out_encoder.

It will be appreciated that the representation of Figure 5, which is altogether evident for a person skilled in the sector after review of the specification, constitutes only one of the possible variant embodiments (which are practically infinite) that enable the same result to be obtained.

The same consideration applies basically also to the diagrams of Figures 6 and 7, which regard, in particular, the modules designated by 12 and 13 in Figure 4.

In the inverting modality (module 12) the signal data_invert and the datum at output from the encoder (data_out_encoder) are taken as input signal, whereas in the non-inverting modality (module 13), instead of the signal data_invert the signal data_in is used.

In both of the cases of Figures 6 and 7 at input to the module 11 or 13 there is present an EX–OR block I2a, I3a designed to operate bit by bit on two inputs.

The diagram of Figure 8, corresponding to an embodiment of the comparison module 14, is aimed at representing the two corresponding signals of hamm_inv and hamm_noinv, which arrive, respectively, from the modules 12 and 13, as well as the signal inv_encoder coming from the output of the flip-flop 16. Within the block 14 is reproduced the HDL description of the corresponding circuit.

The diagram of Figure 9 represents, with a formalism on the whole similar to the one adopted in Figure 5, the diagram of a decoder 20 operating according to the solution previously described with reference to Figure 1.

Also in this case, the reference numbers 2011, 2012 and 2013 indicate respective arrays of EX–OR, NOR (and OR) logic gates, as well as of

pairs of AND and EX–OR logic gates that implement the function of reconstruction of the datum transmitted D, starting from the value B sent on the bus P.

The reference 2014 likewise designates a flip-flop on which the clock signal clk and the reset signal converge. As has already been said with reference to the diagram of Figure 5, the representation of Figure 9, which is altogether evident for a person skilled in the sector, corresponds in actual fact to just one among a number of possible variants that is practically infinite, all of which are able to implement the same logic functions.

The diagram of Figure 10 reproduces the structure of one embodiment of an encoder operating according to the variant described with reference to the flowchart of Figure 2.

It will be appreciated that the diagram is substantially similar to the one represented in Figure 4, so that elements that are identical or functionally equivalent to the ones already represented in Figure 4 are designated with the same reference numbers, which also renders superfluous any repetition herein of the corresponding description.

The main difference between the diagram of Figure 10 and the diagram of Figure 4 is represented by the different structure of the module 11, which is designed to generate, in addition to the signal data_invert also the signal marc_MSb, which, transferred to the comparison block 14, is used for encoding the bit designed to convey the information INV regarding the possible recourse to the traditional bus-inverter technique, should the comparison step 106' of Figure 2 have detected a difference (flags set in the steps 114 and 116).

The diagrams of Figures 11, 12 and 13 reproduce, with a formalism altogether equivalent to the one adopted previously in Figures 5, 8 and 9, the structure of the module 11, as well as of the comparison module 14 and again of the corresponding decoder 20 in the case where the embodiment described in the flowchart of Figure 2 is used. There will be noted, in the diagram of Figure 13, the presence of an additional block, designated by 2014' and designed specifically to

decode the signal INV (inv_decoder) in order to see again whether this assumes the value 0, the value 0.5 or the value 1. The implementation of such a block is evident for a person skilled in the sector after reviewing the specification.

It will moreover be appreciated that the solution described, illustrated as applied, starting from the most significant bit (MSB) of the signal D(t) and of the signal B(t–1), may be applied starting also from the least significant bit (LSB), namely starting either from the most significant bit or from the least significant bit and then proceed towards the inner bits the datum. The same technique may be also applied starting from any other bit, for example the central one, moving towards the left or towards the right, or again in both directions.

Basically, the solution described above corresponds to the identification of a subset of bits identified by a marker bit or marker, with the possibility of applying to the subset thus identified any technique for reducing the switching activity, with the added possibility, for the decoder, of identifying the marker bit, and hence the set of bits subjected to encoding precisely because the marker bit is the first bit in the orderly sequence of comparison between D(t) and B(t–1) to have been subjected to said treatment.

Further improvement of the bus-inverter technique may be achieved by redefining the output in the case where the switching activity of the encoded datum is equal to the switching activity of the non-encoded datum. This innovative solution, albeit finding a preferential application in a context such as the one described previously (use of a marker bit or marker), can be applied also to other encoding techniques, including bus-inverter (BI) techniques of a more traditional type.

In particular, the embodiment described herein detects whether the switching activity achieved by sending the encoded datum is equal to the switching activity achieved with the non-encoded datum, by sending in this case the non-encoded datum and setting the signal INV equal to 0.

In fact, if the switching activity coincides in the two cases, the global switching activity is in any case reduced if the value of the bit INV is left unaltered, i.e., if INV = 0, and the non-encoded datum is sent, maintaining INV always at 0, whereas if INV is equal to 1, then the encoded datum is sent, maintaining INV always at 1.

In other words, instead of assigning to INV a value equal to 0, which may require INV to pass from 1 to 0 if its preceding value was 1, INV is left with the same value that it already had, when the datum was transmitted; consequently, since, as has already been said, the same value of SA is obtained.

Basically, the solution described may be expressed in the following terms:

$$(B(t), INV(t)) = (D(t), 0) \text{ if } H(D(t), B(t-1)) < n/2$$
$$(D(t),0) \quad \text{if } H(D(t), B(t-1)) = n/2 \ \& \ INV = 0$$
$$(NOT(D(t)), 1) \quad \text{if } H(D(t), B(t-1)) = n/2 \ \& \ INV = 1$$
$$(NOT(D(t)), 1) \quad \text{if } H(D(t), B(t-1)) > n/2$$

where B(t) designates the datum that travels on the bus at the instant t and D(t) is the datum that it is intended to send at the instant t; INV designates the value of the additional bit designed to indicate to the receiver whether the datum sent is encoded (inverted, in the example considered herein) or not, and n designates the dimension in number of bits of the bus (without additional line or bit); and the symbol NOT(.) designates the operation of encoding (inversion).

Figure 14 is a flowchart illustrating operation of an encoder in accordance with the present invention. At step 100 the process starts and proceeds to step 120. At step 120 a signal to be transmitted is encoded, for example, by using the process illustrated in Figure 1 or the process illustrated in Figure 2 or any other conventional encoding technique. At step 122, the switching activity associated with transmitting the signal in encoded format is compared to the switching activity associated with transmitting the signal in non-encoded format. If the switching activity associated with transmitting the signal in encoded

format is equal to the switching activity associated with transmitting the signal in non-encoded format, the answer at step 122 is YES and the process proceeds to step 124. Otherwise, the answer at step 122 is NO and the system proceeds to step 126, where the signal is transmitted in an encoded format.

At step 124 the switching activity for transmitting a control signal is compared for the case where the signal to be transmitted is transmitted in an encoded format and the case where the signal to be transmitted is transmitted in a non-encoded format. If the switching activity for transmitting the control signal is greater in the case where the signal to be transmitted is transmitted in a non-encoded format, the answer at step 124 is YES and the system proceeds to step 126, where the signal is transmitted in an encoded format. Otherwise, the answer at step 124 is NO and the system proceeds to step 128, where the signal is transmitted in non-encoded format.

Of course, without prejudice to the principle of the invention, the details of implementation and the embodiments may be amply varied with respect to what is described and illustrated herein, without thereby departing from the scope of the present invention, as defined in the attached claims.

It will be appreciated that the solutions described herein as being implementable at the level of specific hardware circuitry, are suitable also for implementation at a software level by means of processing circuits of a general-purpose type appropriately programmed with a computer product which, when run on the said hardware of a general-purpose type, determines the implementation of the solution according to the invention.